FPGA 实验
项目创建、编译和下载

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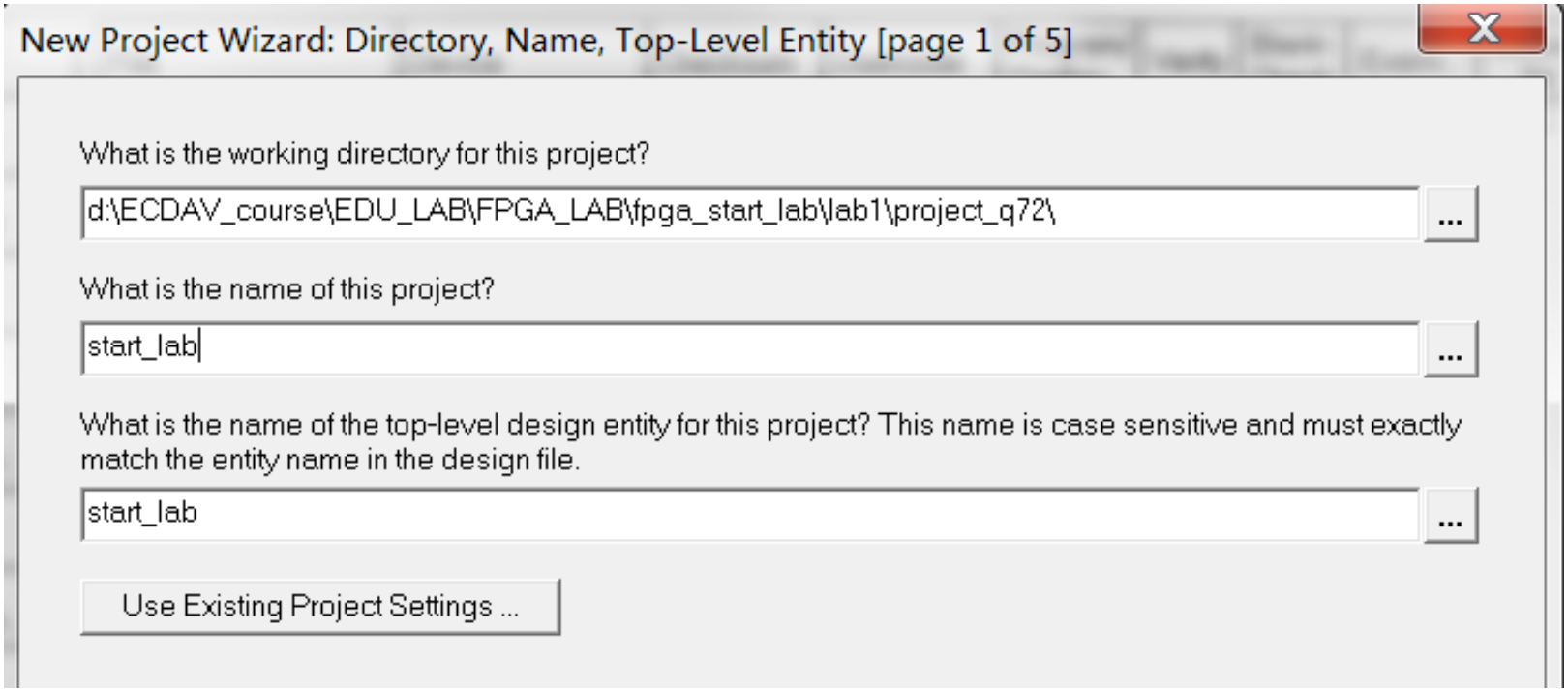
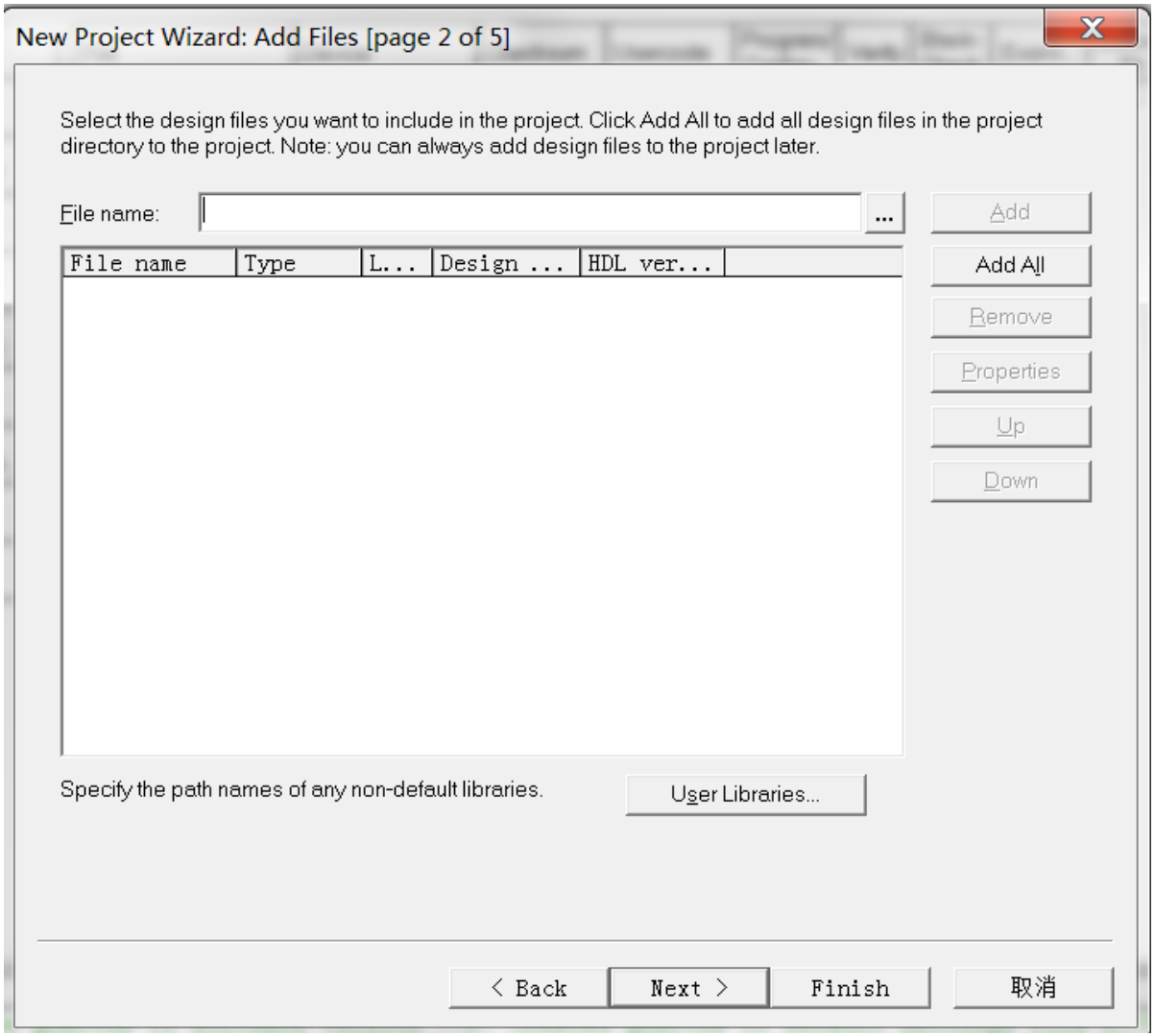
新建项目

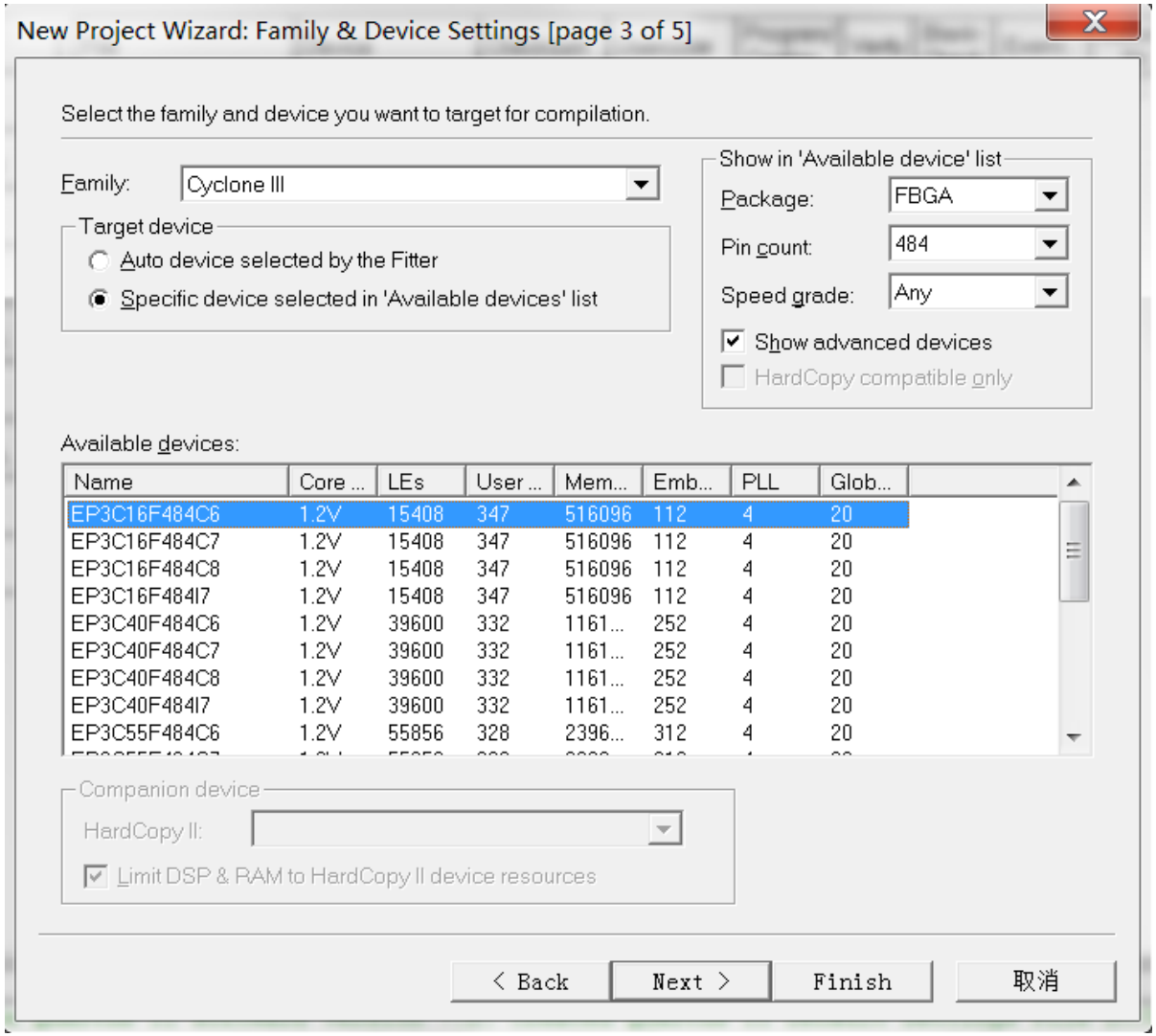


- 填写项目名称和顶层设计的名称
- 最好填写成一样

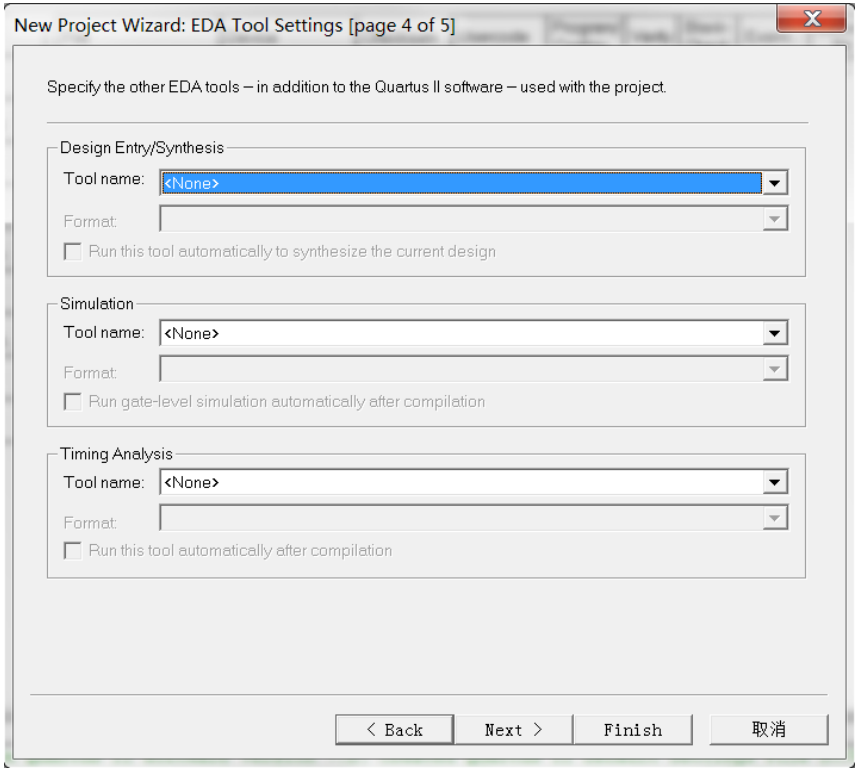
先不用添加文件

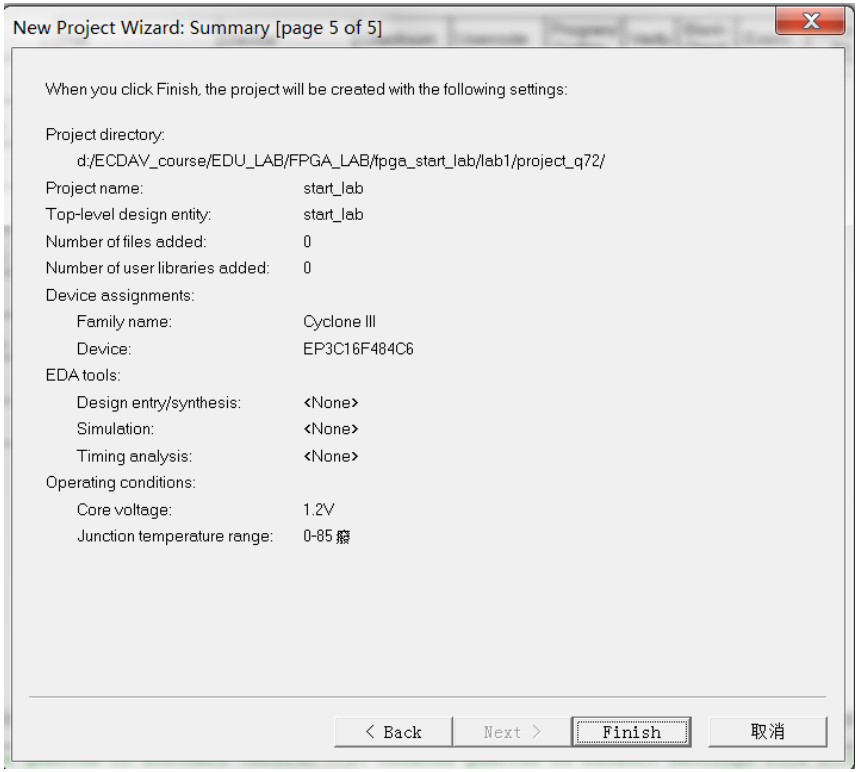

New Project Wizard: Add Files [page 2 of 5]
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project. Note: you can always add design files to the project later.
File name:
...
Add
Add All
Remove
Properties
Up
Down
File name
Type
L...
Design ...
HDL ver...
Specify the path names of any non-default libraries.
User Libraries...
< Back
Next >
Finish
取消

选择电路板对应的FPGA芯片
下图为选择DE0开发板对应芯片

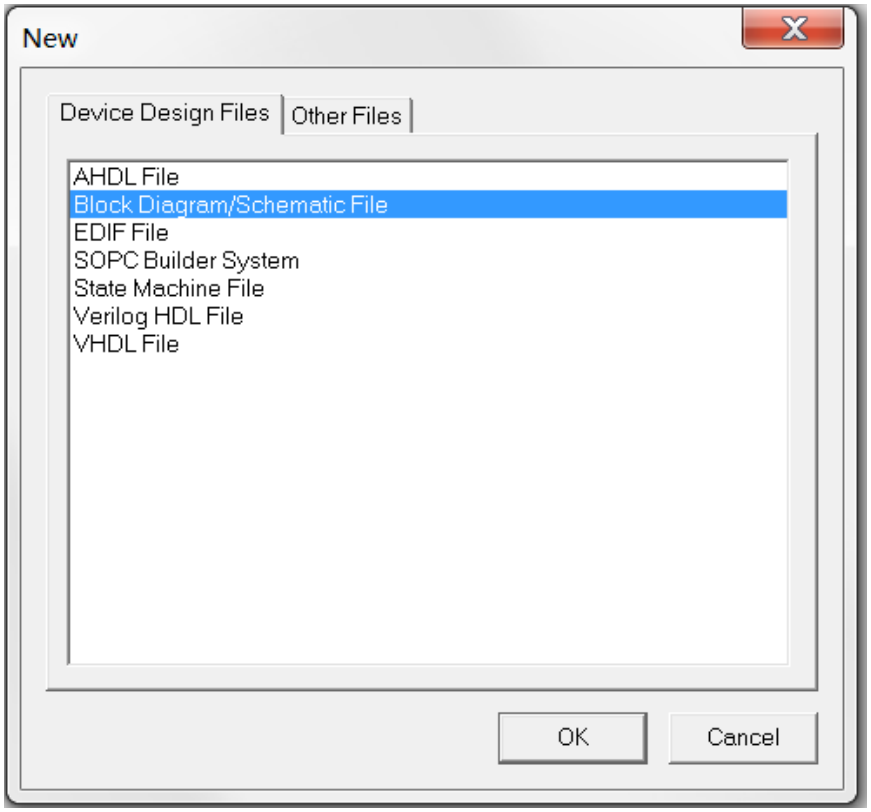


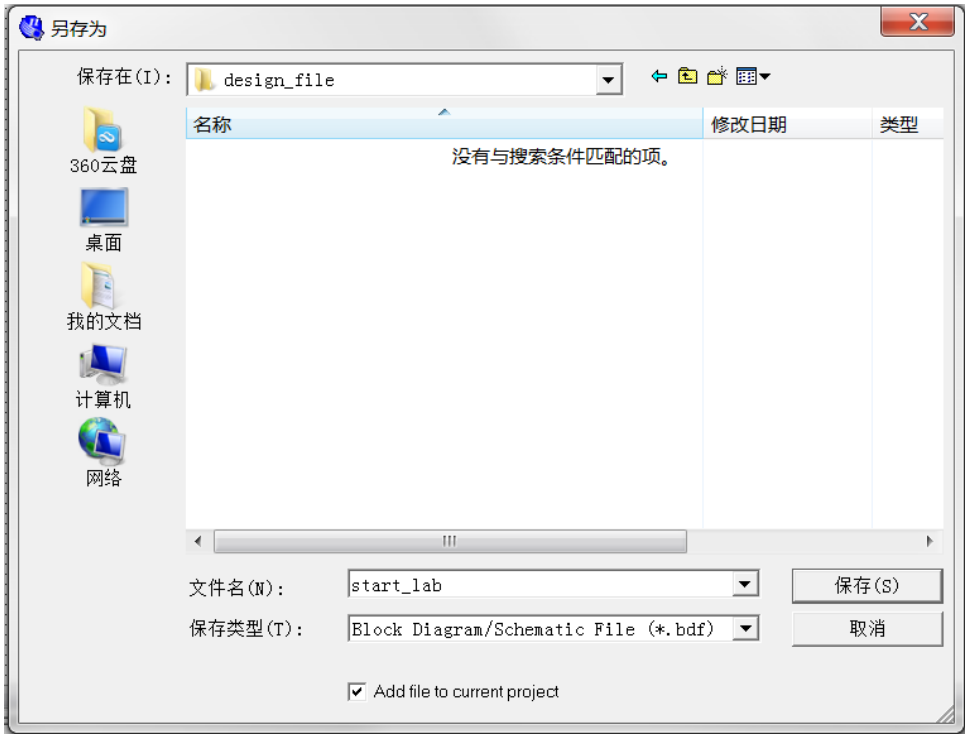
后续步骤，直接Next到Finish





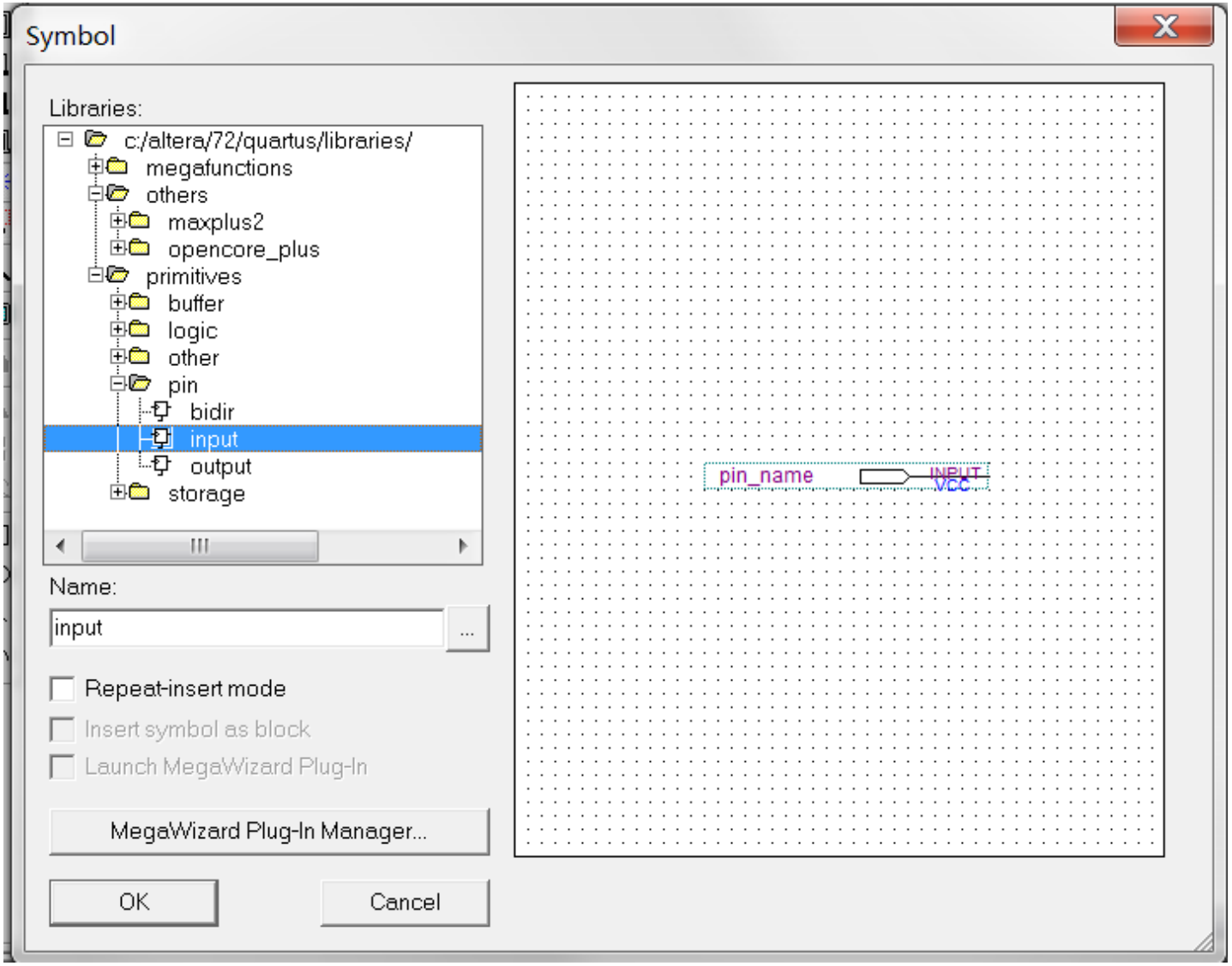
新建一个BDF 文件



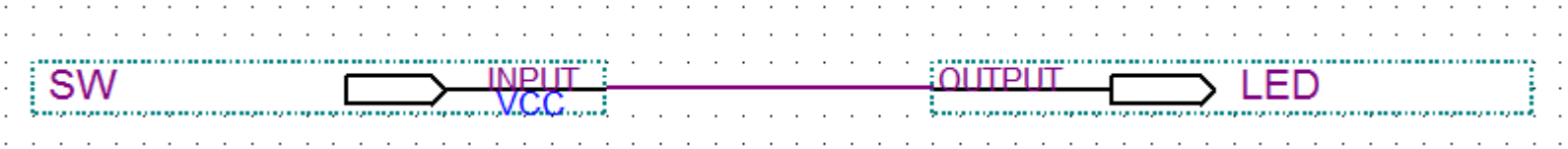


- 然后另存文件
- 注意文件名和顶层设计的名称保持一致

双击BDF文件空白处，放入一个input管脚

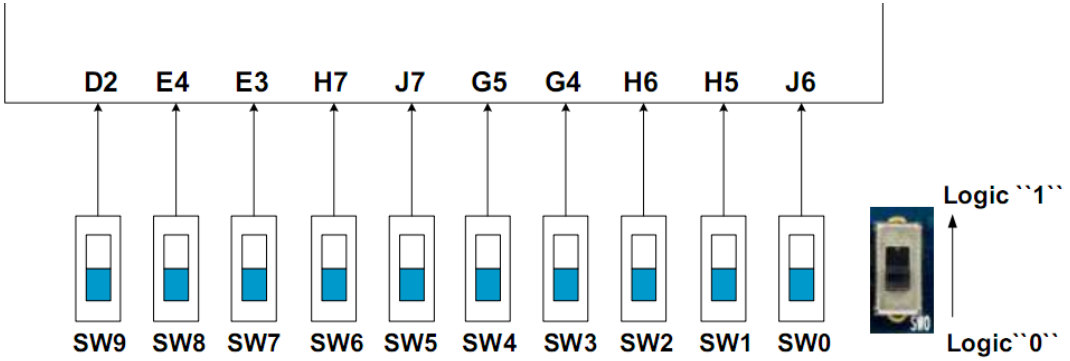


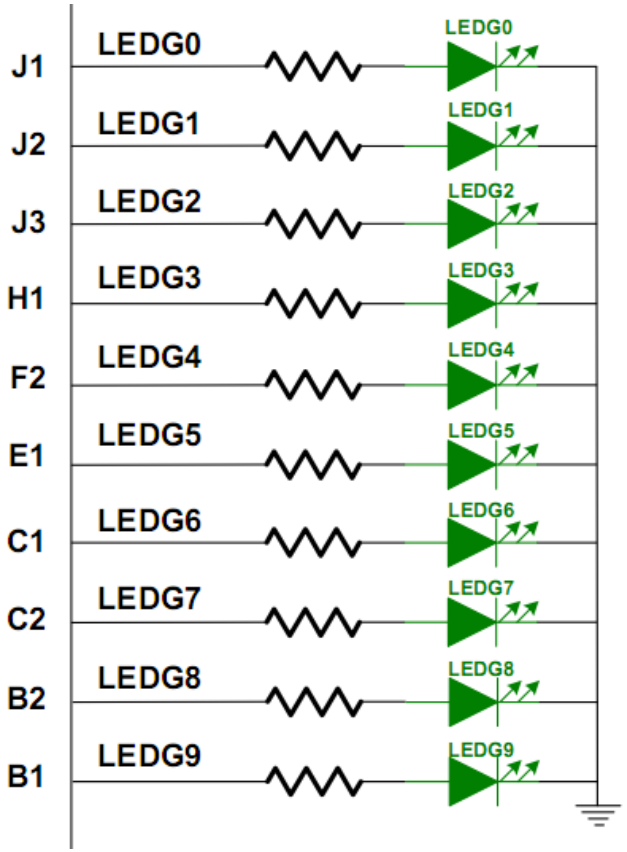
再放一个OUTPUT，和INPUT相连接，设定管脚名称



- 到此，我们设计了一根可编程的导线

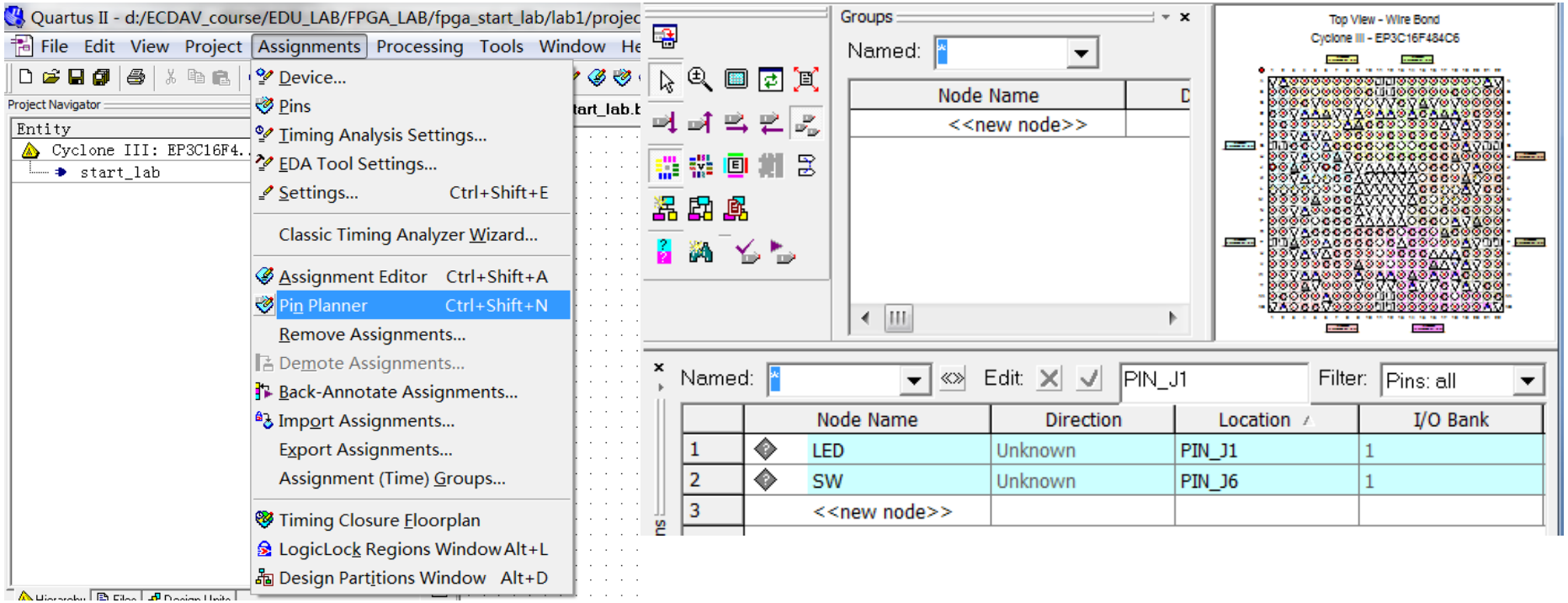
查阅DE0手册中的管脚对应





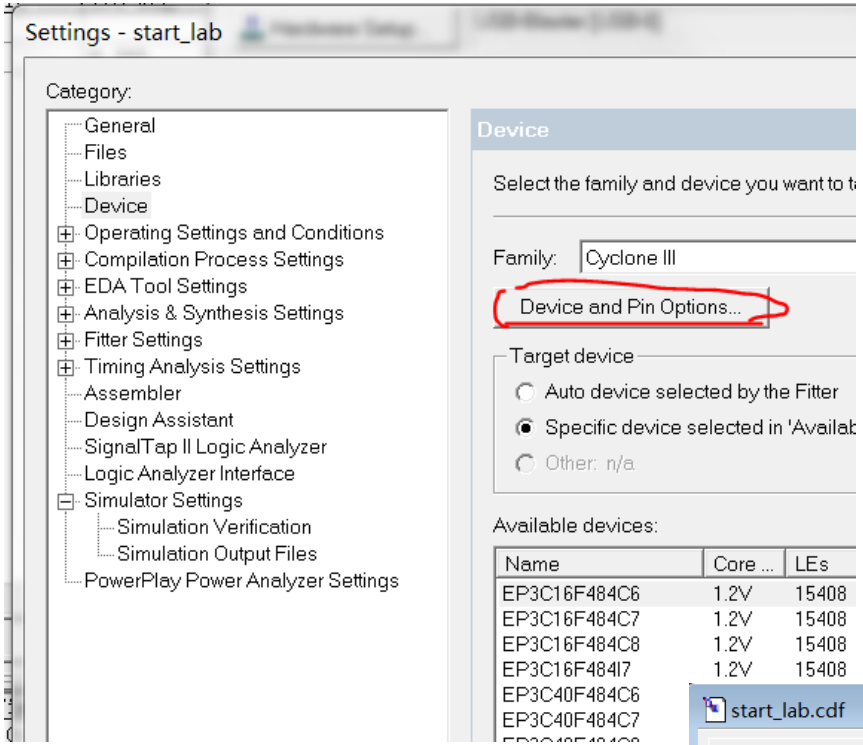
- 可以查阅到拨码开关和LED灯，和FPGA管脚编号的对应关系。

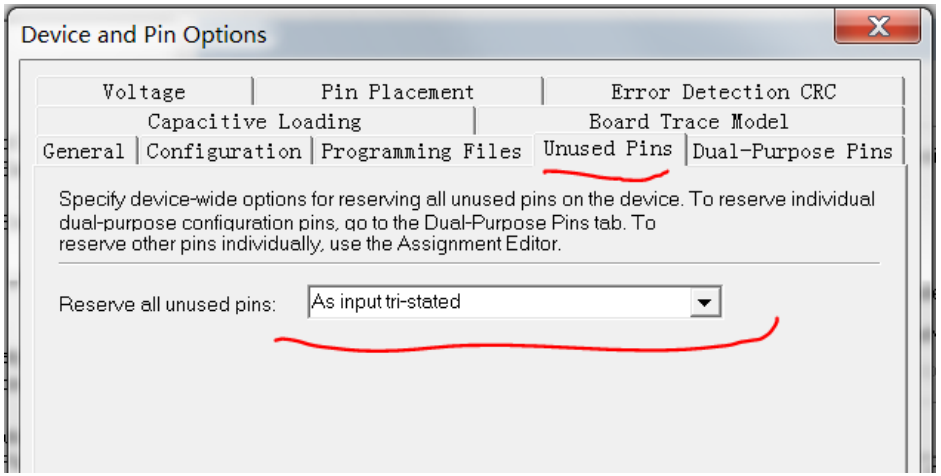
指派管脚



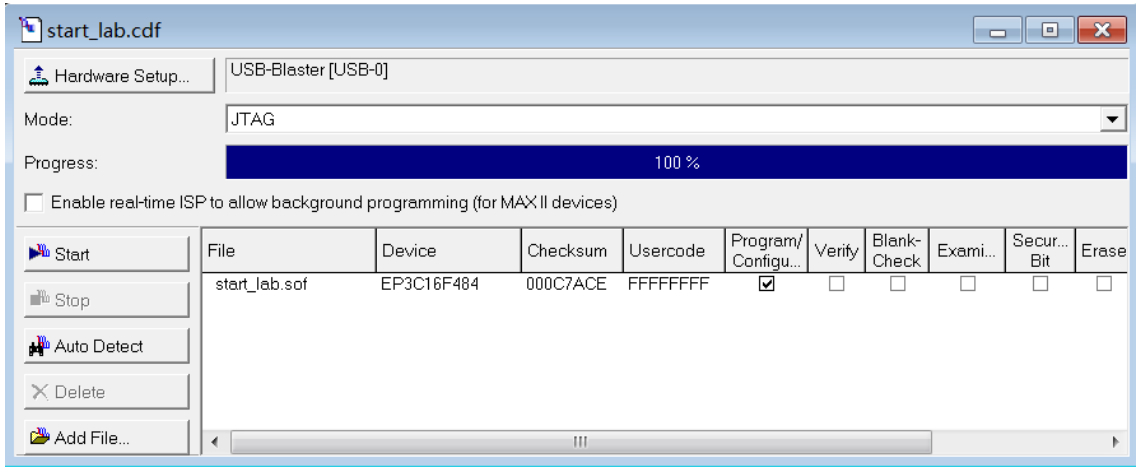
- 设定信号名称和管脚的对应关系

设定不用的管脚为三态





- 然后编译 并下载



- 拨动开关，
- 观察LED亮灭

学生实验

- 仿照本实验，请完成以下任务
  - 用1个拨码开关控制所有的LED灯亮灭